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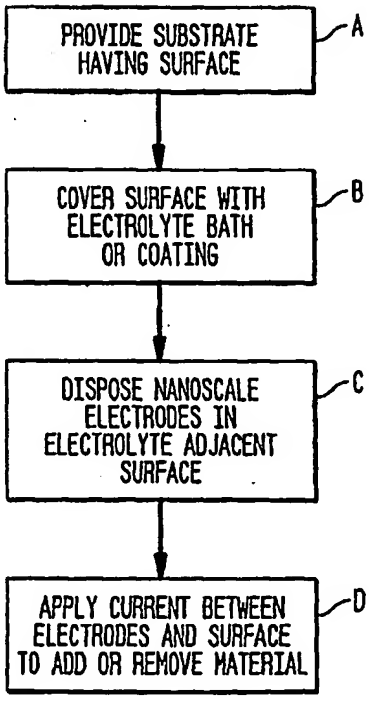

(57) Abstract: In accordance with the invention, a surface of a substrate is patterned by the steps of providing the substrate, covering the surface with electrolyte, and disposing at least one nanoscale electrode in the electrolyte adjacent the surface. A current is then applied between the electrode and the substrate to electrolyically deposit material on or remove material from the surface. The material is deposited or removed in a pattern dependent on the pattern, movement and shape of the nanoscale electrodes. Apparatus for this process and novel products therefrom are also described.

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HIGH RESOLUTION ELECTROLYTIC LITHOGRAPHY, APPARATUS THEREFOR AND RESULTING PRODUCTS

Cross Reference to Related Applications

This application claims the benefit of U.S. Provisional Application Serial No. 60/461,477 filed on April 9, 2003 by Sungho Jin and entitled "Electrolytic Nanolithography Process, Tools for Such Process, and Articles Produced by Such Process", which is incorporated herein by reference.

Field of the Invention

This invention relates to lithography and, in particular, to a method of high resolution lithography using nanoscale electrodes for electrolytic deposition or removal on a substrate. It further includes tools to facilitate this process and novel products made thereby.

Background of the Invention

Lithographic processes are crucial for the manufacture of many semiconductor, optical and nanoscale devices. Lithographic processes are used to create patterned areas on the surface of a substrate which, in turn, can be further processed as by etching, doping, metallizing, growing or other processing to form the features of a desired component, circuit or other device.

The relentless competitive pressure to increase the functionality of such devices has required smaller and smaller patterns. As a consequence, manufacturers are pressing the limits of conventional optical and electron beam lithography. Optical lithography forms a pattern by exposing a photoresist to light through an exposure mask. As is well known, optical lithography is limited by the wavelength of the exposure light. Shorter wavelength light, now in the ultraviolet range, is being used to expose smaller patterns, but the shorter the wavelength, the more complex and expensive the equipment required to generate the light and pattern the substrate.

Electron beam lithography (e-beam lithography) forms a pattern on a resist-covered substrate by projecting an electron beam line-by-line onto the resist to form the pattern. However e-beam lithography is limited in resolution by the need for special stencil masks and, because of its line-by-line exposure, is too limited in speed for satisfactory throughout in manufacturing. In addition, e-beam lithography tools are complex and very expensive.

Accordingly there is a need for simpler, faster and less expensive processes and tools for high resolution lithography and for products that can be made thereby.

Summary of the Invention

In accordance with the invention, a surface of a substrate is patterned by the steps of providing the substrate, covering the surface with electrolyte, and disposing at least one nanoscale electrode in the electrolyte adjacent the surface. A current is then applied between the electrode and the substrate to electrolyically deposit material on or remove material from the surface. The material is deposited or removed in a pattern dependent on the pattern, movement and shape of the nanoscale electrodes. Apparatus for this process and novel products therefrom are also described.

Brief Description of the Drawings

The nature, advantages and various additional features of the invention will appear more fully upon consideration of the illustrative embodiments of the invention described in detail in connection with the accompanying drawings. In the drawings:

Fig. 1 is a schematic block diagram showing the steps in patterning a surface of a substrate in accordance with the invention;

Figs. 2A and 2B illustrate apparatus useful in practicing the method of Fig. 1;

Fig. 3 shows alternative apparatus for practicing the method;

Figs. 4A, 4B, 4C and 4D illustrate an advantageous electrode arrays for the apparatus;

Fig. 5 shows apparatus employing an electrode array;

Fig. 6 illustrates apparatus employing multiple electrode arrays for large area coverage;

Figs. 7A, 7B, 7C and 7D show a technique for fabricating nanoscale electrodes;

Figs. 8A and 8B illustrate the formation of a pattern of active nanoscale electrodes;

Fig. 9 shows an alternative apparatus for electrolytic lithography;

Fig. 10 represents steps in fabricating a nanowire array using the method of Fig. 1;

Fig. 11 illustrates an alternative method of fabricating a nanowire array;

Figs. 12A, 12B, 12C and 12D show different shapes of nanowires that can be formed using the method of Figs. 10 and 11;

Figs. 13A, 13B, 13C and 13D represent the steps involved in fabricating a magnetic recording medium using the method Fig. 1;

Figs. 14A through 14E illustrate an alternative method of making a magnetic recording medium using the method of Fig. 1;

Figs. 15A and 15B schematically show disc storage devices made using the method of Fig. 1;

Figs. 16A through 16D schematically illustrate various types of nanotube arrays;

Fig. 17 is a schematic representation of a microwave amplifier using a nanoemitter array made by the method of Fig. 1;

Fig. 18 is a schematic cross section of a field effect emission display using a nanoemitter array made by the method of Fig. 1;

Fig. 19 is a cross section of plasma display using a nanoemitter array made by the process of Fig. 1; and

Fig. 20 illustrates a quantum dot device made by the process of Fig. 1.

It is to be understood that the drawings are for illustrating the concepts of invention and are not scale.

Detailed Description

A. Basic Method of High Resolution Electrolytic Lithography

Referring to the drawings, Fig. 1 is a block diagram showing the steps involved in the patterning a surface using high resolution electrolytic lithography. The first step, shown in Block A, is to provide the substrate having the surface to be patterned. The substrate advantageously comprises conductive or semiconductive material. The surface is advantageously planar.

The next step, Block B, is to cover the region of the surface to be patterned with an electrolyte. The electrolyte can be for electrodeposition (adding material to the substrate) or for electropolishing (removing material from the substrate). The electrolyte can be in the form of a liquid bath or a thin coating layer. A wide variety of suitable electrolytic baths and coatings are known in the art.

The third step shown in Block C is to dispose one or more nanoscale electrodes in the electrolyte adjacent the surface. The term nanoscale electrode, as used herein, refers to an electrode having at least one lateral dimension (parallel to the surface) less than 500 nm and preferably both orthogonal lateral dimensions each less than 100 nm. If a single electrode is used, it is preferably mounted on a movable support arm to permit writing a pattern. Multiple electrodes can be mounted in stationary or movable arrays or patterns. Shaped electrodes in the form of straight or curved lines of nanoscale width can be used to define patterns. The preferred nanoscale electrodes comprise conductive or semiconductive nanotubes or nanowires. Spacing between the tip of the nanoscale electrode and the surface is advantageously in the range 5 - 1000

nanometers and preferably in the range 10 - 1000 nanometers.

The next step (Block D) is to apply an electrical current between the nanoscale electrode(s) and the substrate to electrolytically add material to the substrate or remove material therefrom. The precise current used depends on the emitting area of the nanoscale electrode, the size of the feature being formed, the desired speed of deposition and the electrolyte being used. Typically the current will be in the range of 0.1 to 100 nanoamperes per nanoemitter.

Fig. 2A illustrates typical apparatus 20 for practicing the process of Fig. 1 comprising a substrate 21 having a surface 22 to be patterned. The substrate 21 is supported in an electrolyte 23A such as a liquid electrolytic bath within a container 24. A nanoscale electrode 25 is disposed in the electrolyte 23A adjacent the surface 22. Here the nanoscale electrode 25 can be a carbon nanotube attached to a movable support arm 26. An optional spacer 27 can also be provided to facilitate close spacing between the electrode 25 and surface 22. A power supply (not shown) can be used to drive electrolyzing electrical current between the electrode 25 and the substrate surface 22. If the electrolyte bath is an electrodepositing bath for the substrate, material regions 28 forming a pattern corresponding to the shape of the electrode emitting surface or its locus if moved will be electrodeposited on the surface 22. If the bath is electropolishing with respect to the surface, material will be removed from the surface in the corresponding pattern (removal not shown in Fig. 2).

The substrate is desirably electrically conductive or semiconductive. If it is an insulating material, such as quartz, aluminum oxide, or silicon oxide, a thin coating of conductive material such as a coating of copper, can be added to the surface as by electroless deposition. If necessary, the conductive material can be removed after electrodeposition by selective light etching to electrically isolate the electrodeposited features. Advantageous materials for electrodeposition include Cr and iron oxide.

An advantageous nanoscale electrode 25 is a carbon nanotube attached to a microscale Si or Si_3N_4 pyramid 29. Such nanoscale electrodes can be fabricated by the techniques for making similar structures for atomic force microscopy (AFM) reported in J.H. Haforer *et al*, "Growth of Nanotubes for Probe Microscopy Tips", 398 Nature

761 (1999) and S. Wong *et al*, "Carbon Nanotube Tips", 120 Journal of American Chemical Society 603 (1998).

B. Other Embodiments of the Method and Apparatus

Fig. 3 illustrates a variation of the Fig. 2A apparatus wherein the nanoscale electrode 25 is partially embedded in an insulating material 30 with a writing tip exposed in the electrolyte 23A. This embedment can be accomplished by embedding the electrode in a potting material and planarizing the end surface. The advantage of this apparatus is that the added insulating material 30 provides positional and mechanical stability to the nanoscale electrode. The added material permits higher rate movement of the electrode in the electrolyte without bending, positional inaccuracy or risk of breaking. The insulating material can be a polymer or ceramic. The planarizing can be effected by grinding, laser planarization, ion-beam machining or even simple pressing against a flat, non-stick surface (such as Teflon) during cure. The optional spacer 27 can be added to the planarized surface to ensure that the writing tip does not inadvertently crash or scratch the surface 22.

Figs. 4A - 4D show various configurations 40 of nanoscale electrode patterns or arrays that can be substituted for the single nanoscale electrode 25 in the Fig. 2 embodiments. Fig. 4A represents an array 40 of straight nanowires 41A with flat writing tips 42A (The term "nanowires" as used herein generically covers both true nanowires--solid cylinders having diameters less than 500 nm--and true nanotubes--hollow cylinders of comparable dimension). Fig. 4B shows an array 40 of nanowires 41B with sharp tips 42B. Fig. 4C is similar to the configuration of Fig. 4B, except the nanowires 41B are potted in an insulating layer 30. Similarly the Fig. 4D embodiment is similar to the Fig. 4A configuration with potted nanowires 41A of flat-tip.

Carbon nanotubes, silicon nanowires and ZnO nanowires can be electrically conducting or semiconducting, and can be grown in aligned form as shown in Figs. 4A and 4B. See C. Bower et al, "Plasma-induced Alignment of Carbon Nanotubes", 77 Applied Physics Letters 830 (2000), K. B. K. Teo et al., "Uniform Patterned Growth of Carbon Nanotubes without Surface Carbon", 79 Applied Physics Letters 1534 (2001), Y. Tu et al., "Growth of Aligned Carbon Nanotubes with Controlled Site Density", 80

Applied Physics Letters 4018 (2002), C. P. Li et al, "Metal Silicide/Silicon Nanowire from Metal Vapor Vacuum Arc Implantation", 14 Advanced Materials, (2002), E. Yenilmez et al., "Wafer Scale Production of Carbon Nanotube Scanning Probe Tip for Atomic Force Microscopy", 80 Applied Physics Letters 2225 (2002), W. I. Park et al., "Metaloganic Vapor-Phase Epitaxial Growth of Vertically Well aligned ZnO nanorods", 80 Applied Physics Letters 4232 (2002) and M. H. Huang et al., "Room-Temperature Ultraviolet Nanowire Nanolasers", 292 Science 1897 (2001).

Embedding the nanoscale electrode arrays 40 in an insulating material can be accomplished in a number of different ways. Physical vapor deposition can be utilized to deposit dielectric material into the gaps between aligned nanoscale electrodes. For example, magnesium oxide, chromium oxide or aluminum oxide can be deposited by RF sputter deposition or by reactive evaporation in an oxidizing atmosphere. Planarization, as by chemical mechanical polishing, can to produce a flat surface with the writing tips flush with the polished surface. Chemical vapor deposition or evaporation of a potting material, such as silicon oxide or a polymer, can also be utilized, followed by planarization if desired. Alternative to the deposition of potting material, a template may be utilized,. For example, a template of anodized alumina having vertically aligned and triangularly arranged holes (diameters typically in the range of 10 –500 nm) may be filled with conductive materials such as Au, Pt, Pd, Ni or Cu by electrodeposition or chemical vapor deposition. See H. Zeng et al., "Magnetic properties of self-assembled nanowires of varying length and diameter", 87 Journal of Applied Physics 4718 (2000), and Peng et al., "Magnetic properties and magnetization reversal of alpha-iron nanowires deposited in alumina film", 87 Journal of Applied Physics 7405 (2000).

Fig. 5 shows a variation of the Fig. 2A/2B apparatus wherein an x-y array 40 of nanoscale electrodes is attached onto the movable arm 26 in order to achieve simultaneous patterning on several different areas of the surface 22. The motion of the arm determines fabrication of various high resolution features such as nanoislands, nanolines or nanocurves ("Nanoislands" refers to dots of material having an effective diameter of 500 nanometers or less. "nanolines" refers to lines having a width of less than 500 nanometers, and a "nanocurves" are curved nanolines).

Similarly, as illustrated in Fig. 6, a plurality of arrays 40 can be attached onto the movable support arm 26 to achieve simultaneous patterning of the surface 22 over a relatively wide area or many different regions.

There are diverse techniques for fabricating advantageous nanoscale electrodes for the apparatus described herein. A single, isolated nanoscale electrode useful for electrolytic nanolithography can be fabricated by using electron beam lithography to produce a single nano-island of catalyst material (e.g., a Co, Ni or Fe island of 1 – 20 nm diameter). Then a single nanowire such as a carbon nanotube, a Si nanowire, or a ZnO nanowire can be nucleated and grown by chemical vapor deposition (CVD), as described in the references of Bower et al., Teo et al. cited above.

The desired diameter of the nanoscale electrodes is in the range of 1 – 500 nm, preferably 1 – 100 nm, and even more preferentially 2 – 30 nm. The desired gap spacing between the nanoelectrodes is also in the range of 1 – 500 nm, preferably 1 – 100 nm, and even more preferentially 2 – 30 nm. The nanoscale electrodes may be placed in a periodic array or in a specific pre-determined pattern.

Another technique is to physically attach a nanotube onto a probe arm such as an AFM tip, as by adhesives or using carbon deposition. See S. Wong et al., 73 Applied Physics Letters 3465 (1998) and H. Nishijima et al, 74 Applied Physics Letters 4061 (1999). Alternatively, arc welding or solder bonding may be used. See H. Mavoori et al, 78 Applied Physics Letters 2976 (2001).

Figs. 7A through 7B illustrate the steps of another technique which involves predepositing a layer of catalyst material 70 such as Co, Ni, or Fe on a sharp-tip conductor 71 and covering the catalyst with a film of non-catalyst metal 72 (Fig. 7A). The structure is then lightly polished to expose island-shape nanoscale catalyst areas 73 (Fig. 7B). Carbon nanotubes or other nanowires 74 can be grown on islands 73 by the CVD process (Fig. 7C). The nanowire 74 so produced can then be further coated with a dielectric material 75 except the very tip so as to concentrate the electrical current and enhance resolution during electrolytic lithography (Fig. 7D).

For an array of nanoscale electrodes such as shown in Fig. 5, it may be desired

that only certain selected nanoscale electrodes in the x-y matrix array be activated so that the same pattern may be mass produced on many substrates. At least three different ways of achieving such a selectivity are described below.

1) One way of achieving the selectivity is to direct electrical current selectively to the chosen nanoscale electrodes. An array of x-y metallization wiring (conductor stripes) can be deposited on the top surface of the arm 26 of Fig. 5 in such a way that respective conductor stripes make electrical contacts with the top ends of respective nanoscale electrodes. The conductors, which can be made of Cu, Pt, Pd, Au, Al, Cr, can be deposited and patterned in accordance with techniques well known in the art. This approach creates reconfigurable nanoscale electrode system by which any desired nano-pattern can be produced using high resolution electrolytic lithography. This approach is viable when the device to be patterned is relatively small and the number of required nanoscale electrodes is not excessive.

2) Another way of creating a reconfigurable nanoscale electrode system is to provide an x – y array of columns and rows of conductors, electrically isolated from each other, in which the x-conductor and y-conductor at each cross-point are connected by a switch, such as a transistor, so that each cross-point (and hence each nanoscale electrode) can be independently activated/controlled to receive electrical current.

3) Yet another approach to prepare a pattern of active nanoscale electrodes is illustrated in Figs. 8A and 8B. Here x-y metallization wiring 80 is applied on the top surface of the arm (26 of Fig. 5) in such a way that the conductor stripes 81 (shown as black lines) make electrical contacts with the top ends of all the nanoscale electrodes. The conductors can then be selectively opened (disconnected) in such a way that only selected x-y cross points corresponding to the desired activated nano-electrodes remain electrically connected to the power source. The disconnections 82 are shown as a series of white dashes. Such a pattern can be obtained either by direct conductor deposition into such a configuration (e.g., using a shadow mask during evaporation deposition), or by post-deposition lithography or by using focused ion beams to create the disconnections. The desired width of the conductor stripes is in the range of 0.5 – 2 times the diameter of the nanoscale electrode. Using the conductor pattern of Fig. 8A,

one can obtain a corresponding pattern of nanoscale deposits 28 (or holes) as illustrated in Fig. 8B.

Fig. 9 shows an alternative embodiment of apparatus 90 for electrolytic lithography wherein the nanoscale electrodes 25 are oriented horizontally in the electrolyte bath 23A rather than vertically and the substrate 21 is supported vertically. While the previously described vertical electrode orientation provides easier movement of the nanoscale electrode assembly, the horizontal orientation of Fig. 9 provides easier and faster processing as by dipping an electrode/substrate assembly into the bath.

C. Applications - Nanotube and Nanowire Arrays

One advantageous application of electrolytic lithography is in the fabrication of arrays or patterns of nanotubes or nanowires such as emitter arrays. Fig. 10 represents the process. In step 100, the high resolution electrolytic lithography is used to deposit one or more nanoscale catalyst islands on a substrate 21. The islands are composed of catalytic metal, such as cobalt, iron or nickel, that acts as a catalyst in the growth of nanowires or nanotubes. In step 101 the substrate 22 is shown with an array of spaced apart islands 28 grown on the surface 21. In step 102, nanowires or nanotubes 103 are grown from the catalyst islands, as by thermal growth for Si or Ge nanowires or by chemical vapor deposition (CVD) for carbon nanotubes. The nanoscale electrode pattern in 100 can replicate a corresponding pattern of nanoscale islands on the substrate which, in turn, replicates a corresponding pattern of subsequently grown nanotubes or nanowires 103. Each nanotube or nanowire is secured to the substrate by a firmly attached electrolytically deposited catalyst island.

Fig. 11 schematically illustrates another advantageous application in the growth of nanowires or nanotubes 111. Here an array of nanoscale electrodes 25 is slowly moved away from the substrate surface 21 as the nanoscale islands are deposited. The electrochemical deposition continues and nanowires or nanotubes are grown. The optimal speed at which the nanoscale electrodes are moved out depends on the electrodeposition rate (which in turn depends on the types and concentration of the electrolyte involved, local current density applied, fluid agitation, and desired nanowire diameter. The speed can be adjusted using, for example, a computer-controlled stepper

motor assembly. By moving the electrodes perpendicularly away from the substrate surface, one can fabricate an advantageous array of spaced apart straight nanotubes or nanowires that extend perpendicular to the substrate. Again each nanotube or nanowire has a firm electrolytically deposited attachment to the substrate.

The advantage of spaced apart arrays of straight emitters can be seen by reference to Figs. 16A through 16D. Typical aligned nanotubes 111 are fabricated in a dense forest configuration, Fig. 16A, which basically wastes the unique, high-aspect-ratio, field-concentrating characteristics of individual carbon nanotubes because of the undesirable electric field shielding. The locally bundled configuration of Fig. 16B is better than the forest structure of Fig. 16A. However, the most desirable structures for field emission are nanotubes (or nanowire in general) that are highly aligned but spaced substantially apart from each other as shown in Fig. 16C Slightly less preferable is the structure of Fig. 16D where small groups of highly aligned nanowires are spaced apart.

The nanowires do not have to be straight. By employing nonlinear movement of arm 26, e.g. zig-zag, spiral, or rectangular nonlinear movement, unique-shaped nanowires can be synthesized. Figs. 12A-12D illustrate straight, zig-zag, spiral and crenellated (rectangular spiral)nanowires that can be grown by corresponding movement of the arm 26. The zig-zag and spiral nanowires (Figs. 12B, 12C, 12D) are mechanically more resilient and compliant. They can be useful for device applications where large effective elastic modulus is desired, such as in some MEMS (micro-electro-mechanical systems) or NEMS (nano-electro-mechanical systems). Sharply bent corners of carbon nanotubes (and nanowires in general) have crystal defects and can serve as heterojunctions which can have semiconducting properties useful for diode or field-effect transistor applications. The zig-zag or rectangularly bent nanowires thus prepared (Figs. 12B and 12D) have one or a multiplicity of such sharply bent corners.

The method and apparatus can also be useful for preparing ultra-high-density nanoscale circuits and devices. The lateral movement of the nanoscale electrodes can produce nano lines and curves of deposited conductors such as Cu, Co, W, Al as well as oxide lines and curves. If operated in a subtractive mode, high resolution electrolytic lithography can produce electropolish etched nano-lines and curves. In an alternative

processing approach, especially if there is a need for nanolithography on surfaces, such as Si or SiO_2, that are difficult to electrolytically pattern, the additive or subtractive nano dots, lines and curves can conveniently be utilized as a mask for subsequent chemical or plasma etch patterning. Each dot, line or curve has a firm electrolytic attachment to the surface 21.

For high-speed preparation of nano patterns, simultaneous use of multiple nanoscale electrodes is preferred. In order to produce lines or curves, instead of islands, the electrolytic processing is intentionally carried out with the nanoscale electrode at a higher than normal height above the substrate. The divergence of electrical current from the nanoscale electrode tips to the substrate connects the islands and produces lines, albeit at the expense of some loss in resolution. By selectively actuating only desired nanoscale electrodes, any desired nanoscale pattern can be generated.

Turning now to specific products, the high resolution electrolytic lithography and apparatus described herein can be used to create a variety of devices including ultra-high-density magnetic recording media, compact disk media, microwave power amplifiers, flat panel field emission displays, plasma displays and quantum dot materials and devices.

D. Applications to Magnetic Recording Media

Magnetic information storage is an important part of modern computer technology. Conventional magnetic recording systems such as computer hard disk drives typically use a continuous magnetic thin film on a rigid substrate as the recording medium. Each bit of information is stored by magnetizing a small area on the thin magnetic film using a write head that will provide a suitable writing magnetic field. The magnetization strength and the location of the magnetic bit representing a bit of binary information should be defined precisely to allow a flying magnetic sensor (a read head) to retrieve the written information.

Figs. 13A-13D illustrate stages of fabricating an ultra-high-density recording medium comprising aligned nanoscale magnets. The first step, Fig. 13A, is depositing

island nuclei 28 of magnetic material using high resolution electrolytic lithography (e.g. the process of Fig. 1). The nuclei 28 advantageously have a diameter of less than 100 nm, preferably less than 20 nm, even more preferably less than 10 nm. Once the nano islands are formed, nanowires of magnetic material can be grown vertically from the substrate to form long and aligned magnetic nanowires (nanomagnets 130 of Fig. 13B. One way of obtaining the nanowires 130 is by continued electrolytic nanolithography with the electrodes moving out from substrate 21 in a controlled manner. Alternatively, the nano-islands can be used for other types of nanowire growth. See, for example, US Patent Application No.10/262,462 "Read Head for Ultra-High-Density Information Storage Media and Method for Making the Same" filed by S. Jin on September 30,2002, which is incorporated herein by reference.

The gap spaces between the nanomagnets 130 are then filled with non-magnetic material (131 of Fig. 13C) such Al, Ti, Si, Cu, Mo, Cr or their alloys, polymers, or non-magnetic compounds of oxides, carbides, nitrides, silicides, or borides. In the final step, Fig. 13(D), the top surface 132 of the gap-filled composite structure is polished flat, as by mechanical polishing or by chemical mechanical polishing (CMP). The desired height of the nanomagnet cylinder is in the range of 10 – 5000 nm, and preferably 50 – 500 nm. The desired range of nanomagnet diameter is less than 100 nm, preferably less than 20 nm, and even more preferably less than 10 nm. With the 10 nm size magnetic bit dimension corresponding to each of the nanomagets present in the inventive recording medium, the recording density can be as high as $\sim 10^{12}$ or 1 terabit/square inch.

Figs. 14A-14E illustrate an alternative process of making an ultra-high-density magnetic recording medium. In the first step, Fig. 14A, a periodic array of magnetic nanowires (or nearly periodic or random array if each magnetic bit is to contain more than one nanowires) is formed on a substrate 22 that oxidizes or reduces easily, such as copper. The array of magnetic nanowires (e.g., Co, Ni or Fe) can be formed on the substrate using the process of Fig. 1 to form catalyst nanoislands and growing the nanowires from the nanoislands.

These nanowires are then oxidized, as by heating in an oxygen-containing

atmosphere, to produce an oxide surface (140 of Fig. 14B), which also serves to decrease the diameter of the magnetic core. An exemplary processing is to heat at 400 –700°C for 0.1- 10 minutes in air or oxygen. The top surface of the copper substrate also is oxidized.

In the next step, Fig. 14C, the structure is chemically reduced, as by subjecting it to heat in a hydrogen-containing atmosphere (250 – 400°C for 1 – 100 minutes in pure hydrogen or a hydrogen/nitrogen mixture). While the Cu-oxide is relatively easily reduced to metallic Cu at this low temperature, Co-oxide remains oxidized as it requires a much higher temperature to be reduced. This results in the structure of Fig. 14C. The magnetic nanowires coated with insulating oxide skin are disposed on a conductive substrate.

A gap-filling material 141, (e.g., Cu) can now be electroplated manner (Fig. 14D) without causing undesirable electrodeposition to take place preferentially at the tip of nanowires. Without the protection of the Co-oxide skin, the Co nanowire would have become longer with added Cu electrodeposit material without efficient filling of the gap with Cu. The structure is then polished to have the flat surface 142 of Fig. 14E. The desired range of nanomagnet diameter and length are similar as for the case of Fig. 13.

E. Applications - Physical Data Storage Media

Another type of recording medium widely used for mass information storage is the recording disc (generically used to include compact discs and DVDs). Compact discs (CDs) have been used mostly for read-only memory (ROM) applications, although a rapid progress is being made in the use of writeable CD disc memory technology. Commercially available CDs are usually made of ~ 1mm thick plastic coated with an aluminum layer and a protective plastic coating. The CD contains physical memory in the form of microscopic bumps or recessed holes arranged as a single or continuous spiral track of data. As the CD disc is rotated in the CD player, a laser beam focused by a lens system follows the spiral track and reads the presence or absence of the bumps or holes.

As the bit size in the current CDs is typically larger than about 200 nm, the recording density is less than a few gigabits per square inch. Utilizing electrolytic nanolithography, CD memory bits can be recorded on a disc or on many discs simultaneously using, for example, the multi-electrode array structure of Figs. 5 and 6. The capacity of information storage density in compact disc media can be increased significantly.

Such ultra-high density CD memory bits can be produced by high resolution electrolytic lithography, either by the additive process or by the subtractive process. Fig. 15(A) illustrates a disc substrate with bits 28 formed by the additive process. Fig. 15(B) shows a disc substrate with bits 28A formed by the subtractive process. The information so recorded can be interrogated and read by a CD-ROM reader.

The information bit size of bumps or recessed holes on a CD surface is made extremely fine using a nanoelectrode array. For example, bit size can be of the order of 10 to 50 nm in diameter, giving rise to a recording density of about 40 gigabits to 1 terabits per square inch. The laser optical technique currently available can no longer effectively detect such fine nanoscale features which is well below the wavelengths of the laser beam used. New techniques which can allow the reading of such nanoscale information bits on ultra-high-density CD discs are disclosed in the US Patent Application No.10/261,217 "Read Head for Ultra-High-Density Information Storage Media and Method for Making the Same" filed by S. Jin on September 30, 2002.

F. Applications Using Emitter Arrays - Vacuum Tube Devices

Fig. 17 is a schematic cross-sectional illustration of an exemplary microwave vacuum tube 170 comprising a spaced-apart nanowire cold cathode 171 prepared by the electrolytic lithographic method described in connection with Fig. 10. The device shown is basically a klystrode structure of gridded tube type (other types of gridded tubes include triodes and tetrodes). The tube 170 contains 5 main elements--the cathode 171, a grid 172, an anode 173, a tail pipe 174, and a collector 175. The whole tube is optionally placed in a uniform magnetic field for beam control.

In operation, a RF voltage is applied between the cathode 171 and grid 172 by

one of several possible circuit arrangements. For example, it is possible for the cathode to be capacitively coupled to the grid or inductively coupled with a coupling loop into an RF cavity containing the grid structure. The grid 172 regulates the potential profile in the region adjacent the cathode, and is thereby able to control the emission from the cathode.

The resulting density-modulated (bunched) electron beam 176 is accelerated toward the apertured anode 173 at a high potential. The beam 176 passes by a gap 177, called the output gap, in the resonant RF cavity and induces an oscillating voltage and current in the cavity. RF power is coupled from the cavity by an appropriate technique, such as inserting a coupling loop into the RF field within the cavity. Finally, most of the beam passes through the tail pipe 174 into the collector 175. By depressing the potential of the collector 175, some of the dc beam power can be recovered to enhance the efficiency of the device.

The improved klystrode structure 170 comprising a spaced-apart nanowire cold cathode 171 is a very efficient device because it combines the advantages of the resonant circuit technologies of the high frequency, velocity-modulated microwave tubes (such as klystrons, traveling wave tubes and crossed-field tubes) and those of the grid-modulation technologies of triodes and tetrodes, together with the unique, cold cathode operation using high-current emission capabilities of nanowire field emitters. The cold cathode 171 allows the grid to be positioned very close to the cathode, for direct modulation of the electron beam signals with substantially reduced transit time.

Since efficient electron emission is typically achieved by the presence of a gate electrode in close proximity to the cathode (placed about 1-100 micrometer distance away), it is desirable to have a fine-scale, micron-sized gate structure with as many gate apertures as possible for maximum emission efficiency and minimize the heating effect caused by electrons intercepted by the gate grids. The grid in vacuum tube device 170 can be made of conductive metal, and can have a perforated, mesh-screen or apertured structure so as to draw the emitted electrons yet let the electrons pass through the apertures and move on to the anode. The apertured grid structure can be prepared by photolithographic or other known patterning technique. The desired average size of the

aperture is in the range of 0.5-500 micrometer, preferably 1-100 micrometer, even more preferably 1-20 micrometer. The grid structure can also be in the form of a fine wire mesh screen, typically with a wire diameter of 5-50 micrometer and wire-to-wire spacing (or aperture size) of 10-500 micrometer. The aperture shape can be circular, square or irregular.

Within each aperture area, a multiplicity of optimally spaced-apart nanotube emitters attached on the cathode surface emit electrons when a field is applied between the cathode and the grid. A more positive voltage is applied to the anode in order to accelerate and impart a relatively high energy to the emitted electrons. The grid is a conductive element placed between the electron emitting cathode and the anode. It is separated from the cathode but is kept sufficiently close in order to induce the emission.

The grid can be separated from the cathode either in a suspended configuration or with an electrically insulating spacer layer such as aluminum oxide. The dimensional stability of the grid, especially the gap distance between the cathode and the grid, is important, for example, in the case of unavoidable temperature rise caused by electron bombardment on the grid and resultant change in dimension and sometimes geometrical distortion. It is desirable that the grid be made with a mechanically strong, high melting point, low thermal expansion metal such as a refractory or transition metal. The use of mechanical strong and creep-resistant ceramic materials such as highly conductive oxides, nitrides, or carbides is also possible. The grid is desirably configured to have as much mechanical rigidity as possible.

Field Emission Displays

Fig. 18 schematically illustrates a flat panel, field emission display 180 comprising a spaced-apart emitter array prepared by the electrolytic lithographic method described in connection with Fig. 10. Here, the term "flat-panel display" means a display with a thickness of less than ~10 cm. Field emission displays can be constructed with either a diode design (i.e., cathode-anode configuration) or a triode design (i.e., cathode-grid-anode configuration). The use of grid electrode is preferred as the field emission becomes more efficient. Advantageously this electrode is a high density aperture gate structure place in proximity to the spaced-apart nanowire emitter

cathode to excite emission. Such a high density gate aperture structure can be obtained by lithographic patterning. For display applications, the emitter material (the cold cathode) in each pixel of the display desirably consists of single or multiple emitters

The field emission display 180 comprises a substrate 181 which also serves as the conductive cathode, a plurality of spaced-apart and aligned nanowire or nanotube emitters 182 connected to the conductive substrate, and an anode 183 disposed in spaced relation from the emitters within a vacuum seal. A transparent anode conductor 183 formed on a transparent insulating substrate 184 (such as a glass) is provided with a phosphor layer 185 and mounted on support pillars (not shown). Between the cathode and the anode and closely spaced from the emitters is a perforated conductive gate layer 186. Conveniently, the gate 186 is spaced from the cathode 181 by a thin insulating layer 187. The emitters are firmly secured to the cathode by electrolytic deposition.

In operation, the space between the anode and the emitter is sealed and evacuated, and voltage is applied by power supply 188. The field-emitted electrons from nanowire or nanotube emitters 182 are accelerated by the gate electrode 186, and move toward the anode conductive layer 183 (typically transparent conductor such as indium-tin-oxide) coated on the anode substrate 184. Phosphor layer 185 is disposed between the electron emitters and the anode. As the accelerated electrons hit the phosphor, a display image is generated.

G. Plasma Displays

The spaced-apart and aligned nanowire structure according to the invention is also useful in improving the performance and reliability of flat panel plasma displays. Plasma displays utilize emissions from regions of low pressure gas plasma to provide electrodes within a visible display elements. A typical plasma display cell comprises a pair of electrodes in sealed cell containing a noble gas. When a sufficient voltage is applied between the electrodes, the gas ionizes, forms a plasma, and emits visible and ultraviolet light. Visible emissions from the plasma can be seen directly. Ultraviolet emissions can be used to excite visible light from phosphors. An addressable array of such display cells forms a plasma display panel. Typically display cells are fabricated in an array defined by two mating sets of orthogonal electrodes deposited on two

respective glass substrates. The region between the substrates is filled with a noble gas, such as neon, and sealed.

Fig. 19 schematically illustrates a plasma display cell 190 using a spaced-apart emitter array 191 made by the process of Fig. 1. The cell 190 comprises a pair of insulating plates 192 and 193 separated by dielectric barrier ribs 194. One plate 192 includes an anode 195 that is preferably transparent, and the other includes emitter array 191 comprising a spaced apart array of nanoscale emitters 196 on a conductive or semiconductive substrate 197 to act as a cathode. The plate 192 and 193 can be soda lime glass. The anodes 195 can be a metal mesh or an indium-tin-oxide (ITO) coating. The cathode/substrate 197 can be a metal, such as Ni, W, or stainless steel, or it can be a conductive oxide. A noble gas, such as Ne, Ar or Xe or mixtures thereof, is sealed in the space between the electrodes. Typical spacing between plates 192, 193 is about 200 micrometers.

In operation, voltage from a power supply (not shown) is applied across the electrodes to form a plasma 198 that emits light. The emitters 196 of array 191 emit electrons more easily than conventional emitters, thus allowing the formation of the plasma 198 at relatively low voltages. This facilitated emission greatly reduces the power consumption, simplifies the drive circuitry and permits higher resolution. The emitters are firmly secured to their substrate surfaces by electrolytic deposition.

H. Quantum Dot Materials and Devices

Semiconductor quantum dots are nanoscale islands of semiconductor materials such as Si, GaAs, GaP, InP, CdSe, etc. A quantum dot acts as a box that can hold only a discrete number of electrons. The number of electrons in the quantum dot can be altered by controlling electric fields to a nearby gate. The unique behavior of quantum dots at the extremely small dimension is useful for devices such as single electron transistors, light emitting diodes, photovoltaic cells, logic devices and quantum lasers. Quantum dot materials are conventionally fabricated by colloidal chemistry. See A. P. Alivisatos, 23 Materials Bulletin 18 (February 1998), C. B. Murray, *et al.* 270 Science 1335 (1995). The placement of quantum dot location using the processing of colloidal semiconductor nano particles on a substrate is often imperfect, and the mechanical

adhesion and electrical connection between the nano particles and the substrate which supplies the electrical signals may not be always ideal.

Fig. 20 is a schematic cross section of an exemplary quantum dot device 200 comprising a patterned array of nano islands 201 made by the process of Fig. 1. This particular device 200 comprises a single electron tunneling transistor formed by two pairs of nano islands 201 spaced apart by an electron tunneling gap 202 of about 1-20 nanometers overlying an insulating layer 203 formed on substrate 205. The spaced apart pairs are connected by a conductive line 205 such as Cu or cobalt silicide. Conductive lines 206 can also provide respective contacts to the nano islands that are not connected together.

In operation, the voltage between the connected and unconnected nano islands determines whether or not individual electrons can quantum mechanically tunnel between the non-connected islands and the connected islands. The nano islands are firmly secured to the substrate by electrolytic deposition.

Using the inventive electrolytic nanolithography, quantum dot island structure can easily and efficiently be produced. The advantage of the inventive process using nanoscale electrodeposition is that well adhered and electrically well-contacted quantum dot islands on the substrate surface can be obtained, and that periodically placed, or selective positioned quantum dot distribution on can be achieved. The electrolytic nanolithography can be used to either directly deposit the quantum dot material or just to deposit a catalyst or precursor material in the shape of the islands followed by subsequent chemical or physical vapor deposition selectively on the catalyst islands. For direct quantum dot deposition, either an alloy dot deposition, a two-layer deposition of component elements and alloying heat treatment, or a single metal deposition followed by subsequent doping processing may be utilized to produce alloy quantum dots. Improved nano electronic devices such as single electron transistors, light emitting diodes, photovoltaic cells, logic devices and quantum lasers can be produced using the inventive processing.

It is understood that the above-described embodiments are illustrative of only a few of the many possible specific embodiments which can represent applications of the

invention. Numerous and varied other arrangements can be made by those skilled in the art without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of patterning a surface of a substrate comprising the steps of:

providing the substrate;

covering at least a portion of the surface with an electrolyte;

disposing at least one nanoscale electrode in the electrolyte adjacent the surface; and

applying a current between the electrode and the substrate to electrolytically deposit material on or remove material from the substrate surface.

2. The method of claim 1 wherein the covering comprises immersing the substrate in an electrolyte bath.

3. The method of claim 1 wherein the covering comprises applying a coating layer of electrolyte to the surface.

4. The method of claim 1 further comprising the step of moving the electrode to write a pattern.

5. The method of claim 1 wherein the nanoscale electrode comprises a nanowire or nanotube.

6. The method of claim 1 wherein at the least one nanoscale electrode

comprises a plurality of nanowires or nanotubes disposed in a pattern or in a spaced-apart array.

7. The method of claim 1 wherein the substrate comprises electrically conductive or semiconductive material.

8. The method of claim 1 wherein the at least one nanoscale electrode comprises at least one nanowire or nanotube partially embedded in insulating material.

9. The method of claim 1 wherein the at least one nanoscale electrode comprises a plurality of spaced apart nanowires or nanotubes partially embedded in insulating material.

10. Apparatus for patterning a surface of a substrate comprising:

a support for the substrate, the substrate surface in contact with an electrolyte;

one or more nanoscale electrodes;

a movable support for the one or more electrodes, the electrodes attached to the movable support, and the movable support movable to dispose the one or more electrodes in the electrolyte adjacent the surface of the substrate;

a power supply for supplying electrical current; and

a conducting path connecting the substrate and the one or more electrodes to the power supply for supplying current to electrolytically add or remove material on the surface.

11. The apparatus of claim 10 wherein the movable support is movable parallel to the surface.

12. The apparatus of claim 10 wherein the movable support is movable perpendicular to the surface.

13. The apparatus of claim 10 wherein the one or more electrodes comprise one or more nanowires or nanotubes.

14. The apparatus of claim 10 wherein the one or more electrodes comprise a plurality of nanowires or nanotubes.

15. The apparatus of claim 10 wherein the one or more electrodes comprise a plurality of nanowires or nanotubes disposed in a spaced apart array.

16. The apparatus of claim 10 wherein the one or more electrodes comprises one or more nanowires or nanotubes partially embedded in insulating material.

17. The apparatus of claim 10 wherein the one or more electrodes comprise a plurality of nanowires or nanotubes disposed in a spaced-apart array and partially embedded in insulating material.

18. The apparatus of claim 10 wherein the one or more electrodes comprise a plurality of nanoscale electrodes disposed in a spaced-apart array, and the conducting

path connecting the electrodes to the power supply is switchable to permit the connection or disconnection of selected electrodes.

19. The apparatus of claim 10 wherein the support for the one or more nanoscale electrodes supports the one or more electrodes in a horizontal orientation.

20. A method of fabricating an array or pattern spaced-apart nanoscale islands of material on a surface of a surface of a substrate comprising the steps of:

providing the substrate;

covering at least a portion the surface with an electrolyte;

disposing in the electrolyte adjacent the surface a plurality of nanoscale electrodes configured in a spaced-apart array or pattern; and

applying current between the electrodes and the substrate to electrolytically deposit the spaced-apart nanoscale islands of material on the surface.

21. A method of fabricating an array or pattern of spaced-apart nanowires or nanotubes on a surface of a substrate comprising the steps of:

providing the substrate;

covering at least a portion of the surface with an electrolyte for depositing a material that is a catalyst for the growth of the nanowires or nanotubes;

disposing in the electrolyte adjacent the surface a plurality of nanoscale electrodes;

applying current between the electrodes and the substrate to electrolytically deposit regions of the catalyst material on the surface in the spaced-apart array or

pattern; and

growing the nanotubes or nanowires on the regions of catalyst material.

22. A method of fabricating a straight or curved line on a surface of a substrate comprising the steps of:

providing the substrate;

covering at least a portion of the surface with an electrolyte;

disposing at least one nanoscale electrode in the electrolyte adjacent the surface; and

moving the electrode parallel the surface while applying current between the electrode and the substrate to electrolytically deposit or remove the straight curved line on the substrate surface.

23. An article comprising:

a substrate having a surface; and

disposed on the surface an array or pattern of electrolytically deposited nano islands having effective diameters less than about 500 nanometers.

24. An article comprising:

a substrate having a surface; and

disposed on the surface an array or pattern of electrolytically deposited nanoscale features comprising straight or curved nanolines having widths less than 500 nanometers.

25. An article comprising:

a substrate having a surface; and

disposed on the surface a pattern or array of spaced-apart nanotubes or nanowires grown on a corresponding pattern or array of electrolytically deposited nano islands of catalyst material.

26. An article according to claim 25 comprising a magnetic recording medium including an array of spaced-apart magnetic recording elements partially embedded in nonmagnetic material, wherein the spaced-apart nanotubes or nanowires comprise the magnetic recording elements.

27. An article according to claim 25 comprising a vacuum tube composed of a cathode, a grid, an anode, and a collector, wherein the spaced-apart array of nanotubes or nanowires comprises the cathode.

28. An article according to claim 25 comprising a field emission display including a cathode, a spaced-apart array of electron emitters connected to the substrate, an anode and a phosphor layer, wherein the spaced-apart array of nanotubes or nanowires comprise the electron emitters.

29. An article according to claim 25 comprising a plasma display including a plurality of plasma display cells having spaced-apart electrode pairs sealed with ionizable gas, wherein the spaced-apart array of nanotubes or nanowires comprise the spaced-apart electrode pairs.

30. An article according to claim 23 comprising a quantum dot device including a substrate supporting a plurality of nanoscale islands of semiconductor material, wherein the electrolytically deposited nanoscale features comprise the semiconductor nanoscale islands.

FIG. 1

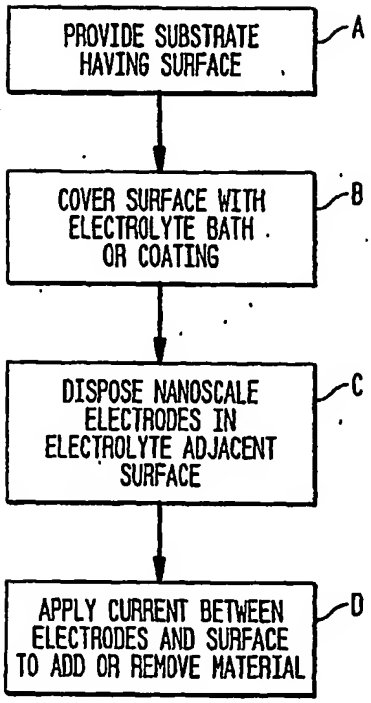

PROVIDE SUBSTRATE HAVING SURFACE
A
COVER SURFACE WITH ELECTROLYTE BATH OR COATING
B
DISPOSE NANOSCALE ELECTRODES IN ELECTROLYTE ADJACENT SURFACE
C
APPLY CURRENT BETWEEN ELECTRODES AND SURFACE TO ADD OR REMOVE MATERIAL
D

FIG. 2A

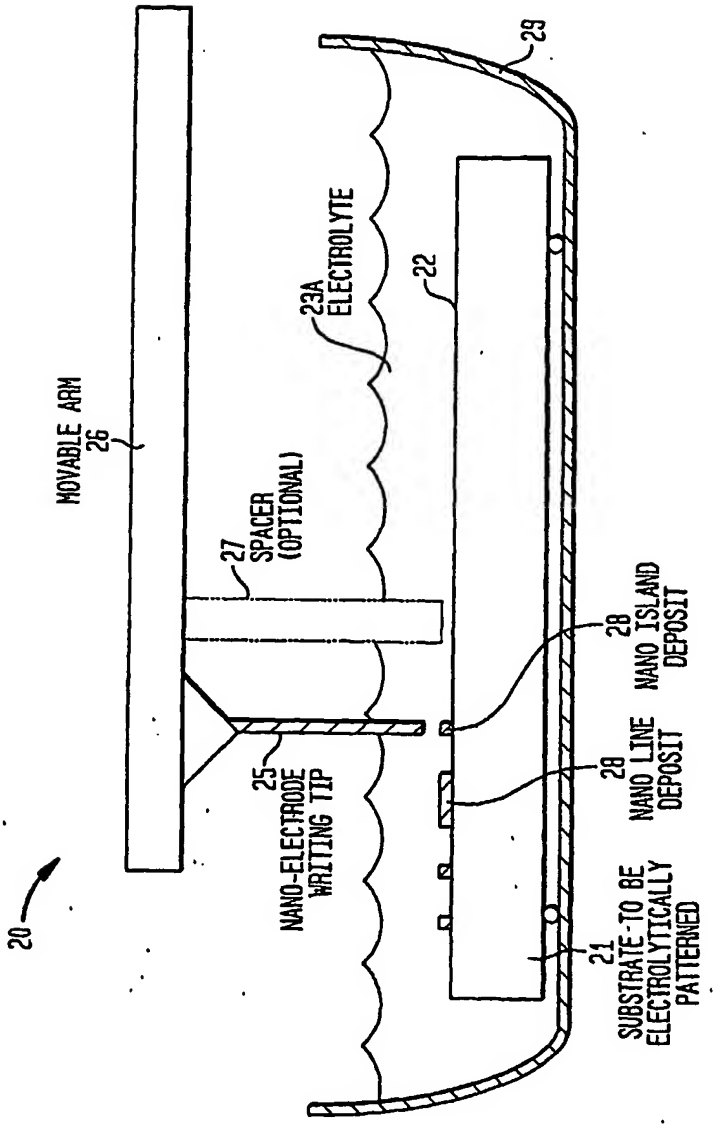

MOVABLE ARM
26
27
SPACER
(OPTIONAL)
23A
ELECTROLYTE
22
29
28
NANO ISLAND
DEPOSIT
28
NANO LINE
DEPOSIT
25
NANO-ELECTRODE
WRITING TIP
21
SUBSTRATE-TO BE
ELECTROLYTICALLY
PATTERNED
20

FIG. 2B

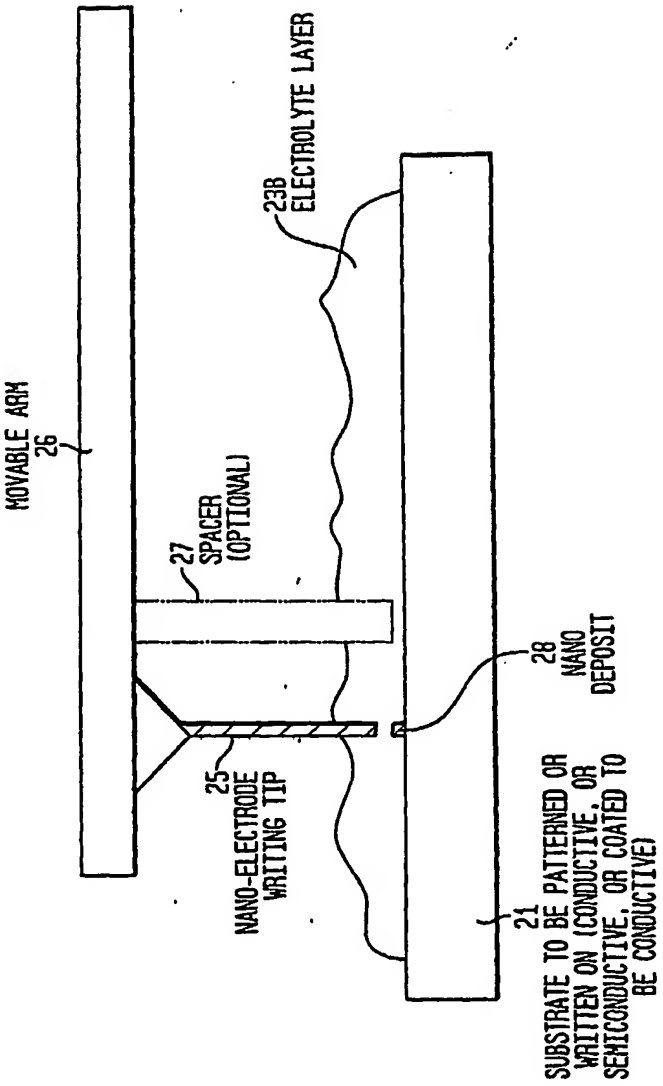

MOVABLE ARM
26
23B
ELECTROLYTE LAYER
27
SPACER
(OPTIONAL)
28
NANO
DEPOSIT
25
NANO-ELECTRODE
WRITING TIP
21
SUBSTRATE TO BE PATTERNED OR
WRITTEN ON (CONDUCTIVE, OR
SEMICONDUCTIVE, OR COATED TO
BE CONDUCTIVE)

FIG. 3

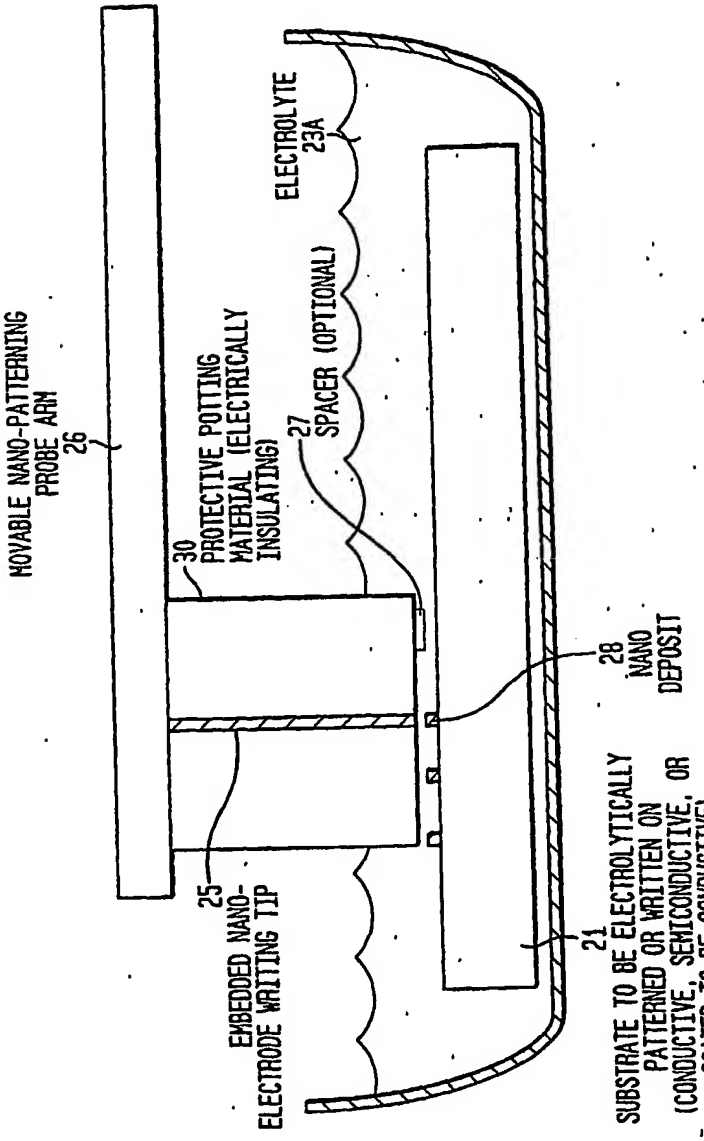

MOVABLE NANO-PATTERNING PROBE ARM
26
30
PROTECTIVE POTTING MATERIAL (ELECTRICALLY INSULATING)
27
SPACER (OPTIONAL)
ELECTROLYTE 23A
28
NANO DEPOSIT
25
EMBEDDED NANO-ELECTRODE WRITING TIP
21
SUBSTRATE TO BE ELECTROLYTICALLY PATTERNED OR WRITTEN ON (CONDUCTIVE, SEMICONDUCTIVE, OR COATED TO BE CONDUCTIVE)

FIG. 4D

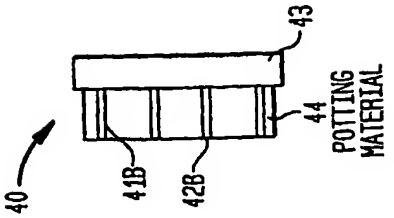


FIG. 4C

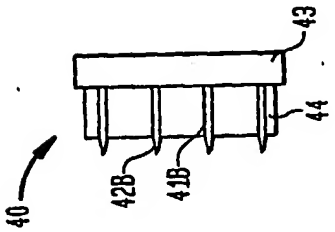


FIG. 4B

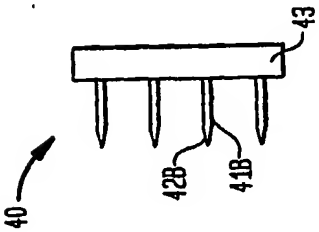
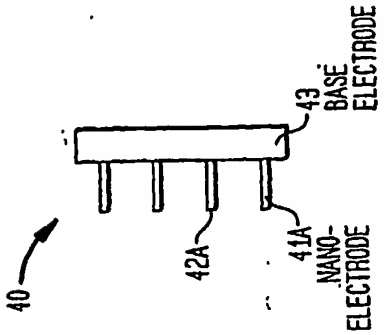


FIG. 4A



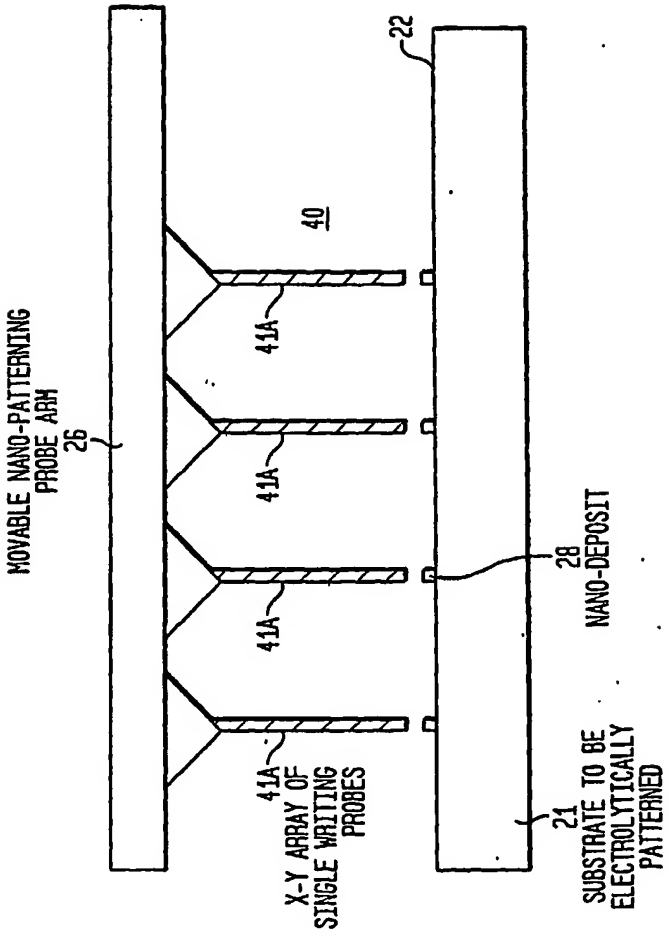
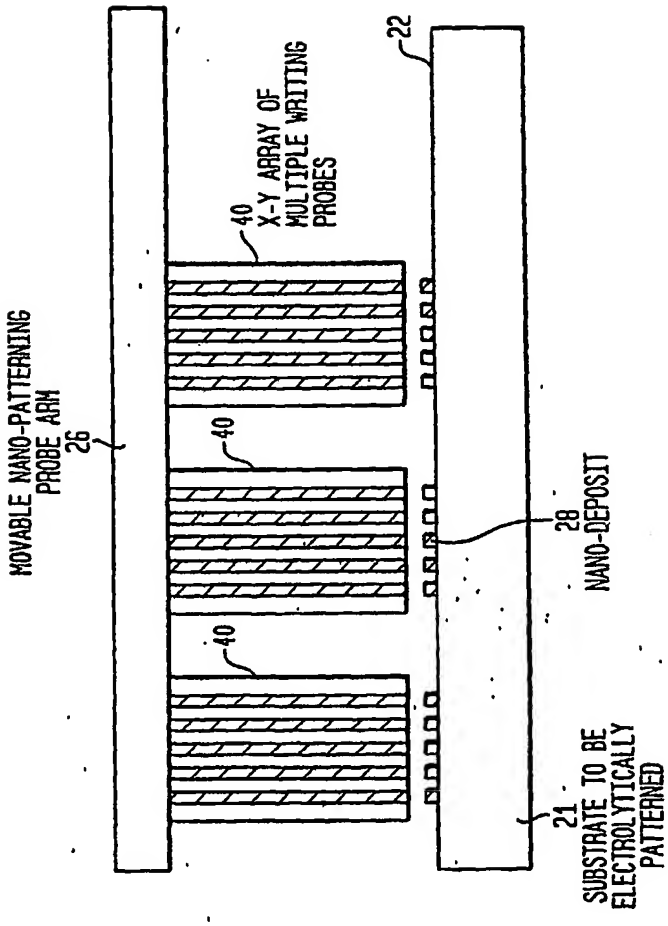

MOVABLE NANO-PATTERNING PROBE ARM
26
40
41A
41A
41A
41A
X-Y ARRAY OF SINGLE WRITING PROBES
22
28
NANO-DEPOSIT
21
SUBSTRATE TO BE ELECTROLYTICALLY PATTERNED

FIG. 5

FIG. 6


MOVABLE NANO-PATTERNING PROBE ARM
26
40
X-Y ARRAY OF MULTIPLE WRITING PROBES
22
40
40
28
NANO-DEPOSIT
21
SUBSTRATE TO BE ELECTROLYTICALLY PATTERNED

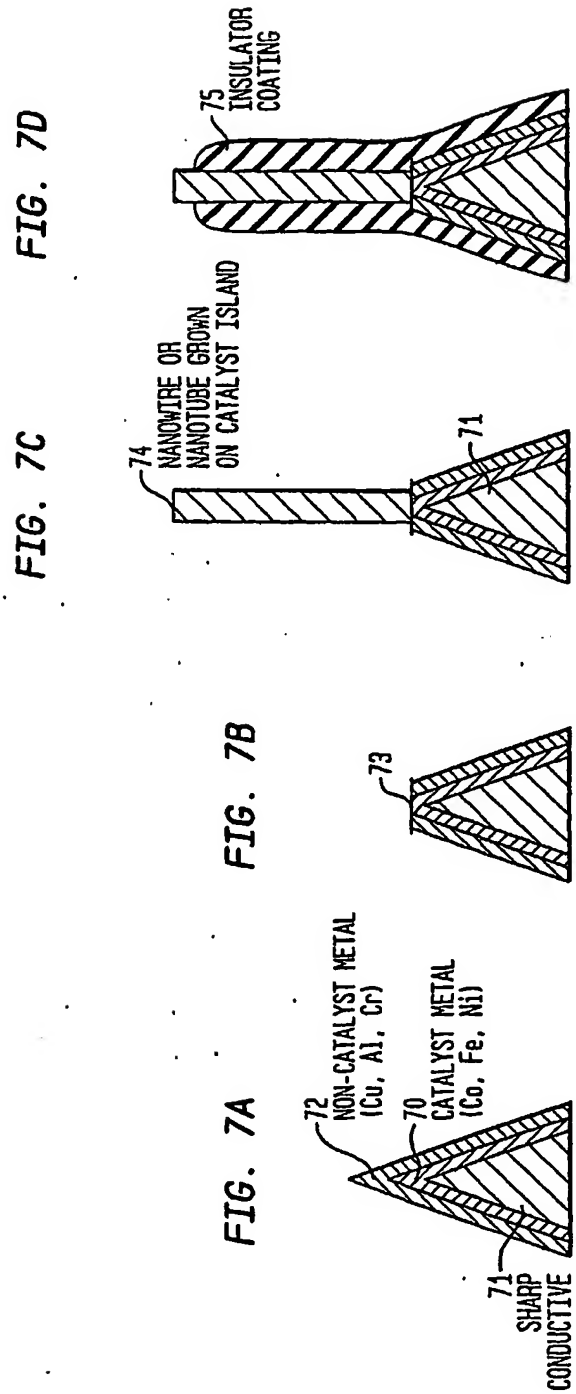


FIG. 7A
72
NON-CATALYST METAL
(Cu, Al, Cr)
70
CATALYST METAL
(Co, Fe, Ni)
71
SHARP
CONDUCTIVE
TIP
FIG. 7B
73
FIG. 7C
74
NANOWIRE OR
NANOTUBE GROWN
ON CATALYST ISLAND
71
FIG. 7D
75
INSULATOR
COATING

FIG. 8A
SELECTION OF ELECTRODES TO BE ACTIVATED BY WIRING REARRANGEMENT IN THE UPPER PART

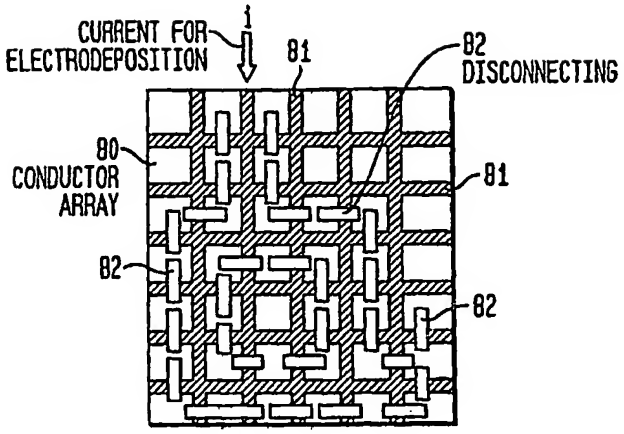


FIG. 8B
RESULTANT NANO-DEPOSIT PATTERN ON SUBSTRATE

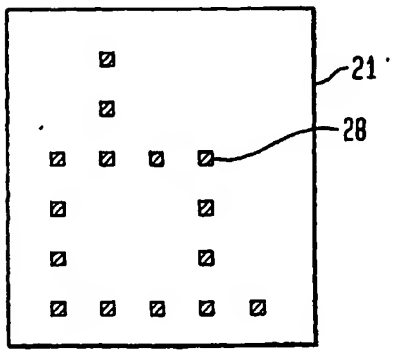


FIG. 9

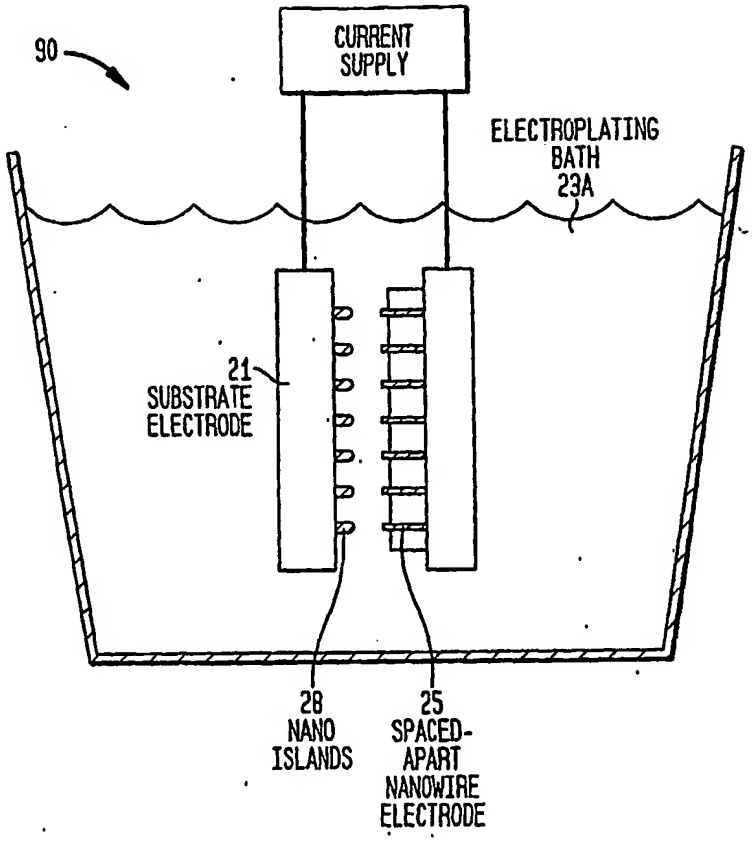

90
CURRENT SUPPLY
ELECTROPLATING BATH 23A
21
SUBSTRATE ELECTRODE
28
NANO ISLANDS
25
SPACED-APART NANOWIRE ELECTRODE

FIG. 10

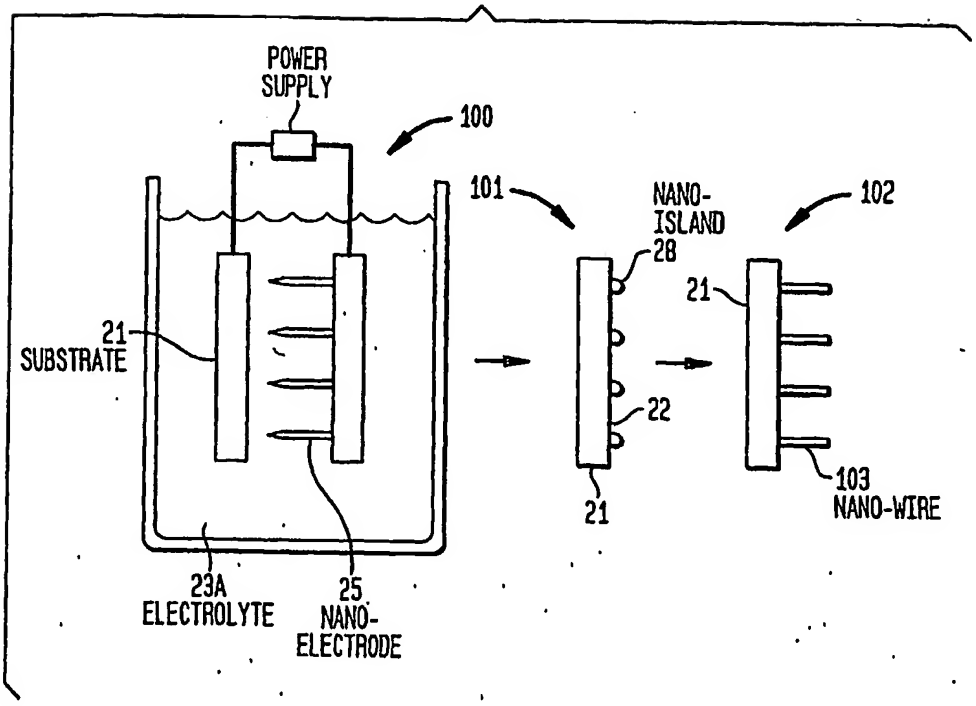
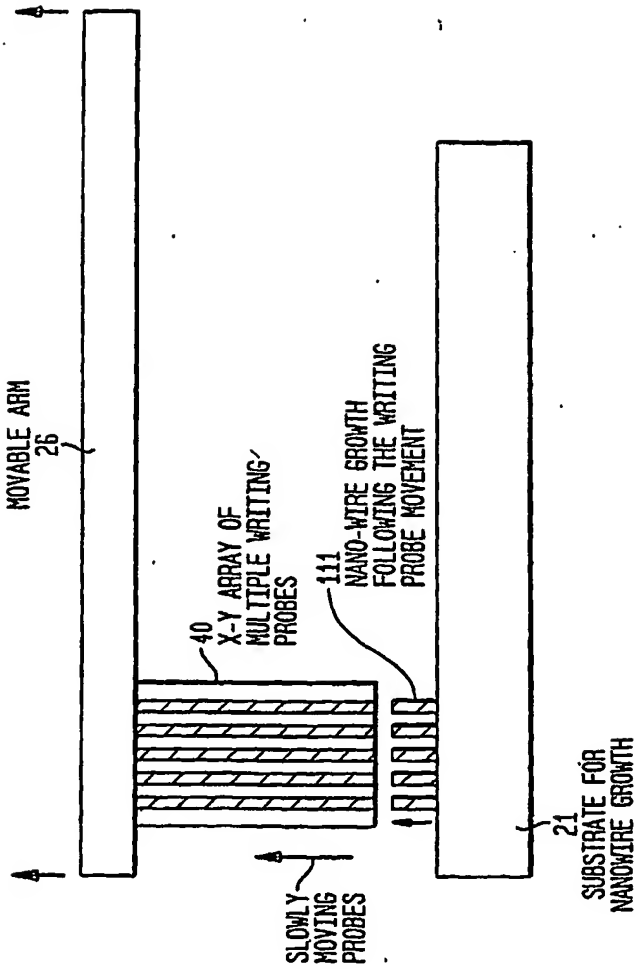

POWER SUPPLY
100
101
NANO-ISLAND
28
102
21
21
SUBSTRATE
22
21
103
NANO-WIRE
23A
ELECTROLYTE
25
NANO-ELECTRODE

FIG. 11


MOVABLE ARM
26
40
X-Y ARRAY OF
MULTIPLE WRITING
PROBES
111
NANO-WIRE GROWTH
FOLLOWING THE WRITING
PROBE MOVEMENT
21
SUBSTRATE FOR
NANOWIRE GROWTH
SLOWLY
MOVING
PROBES

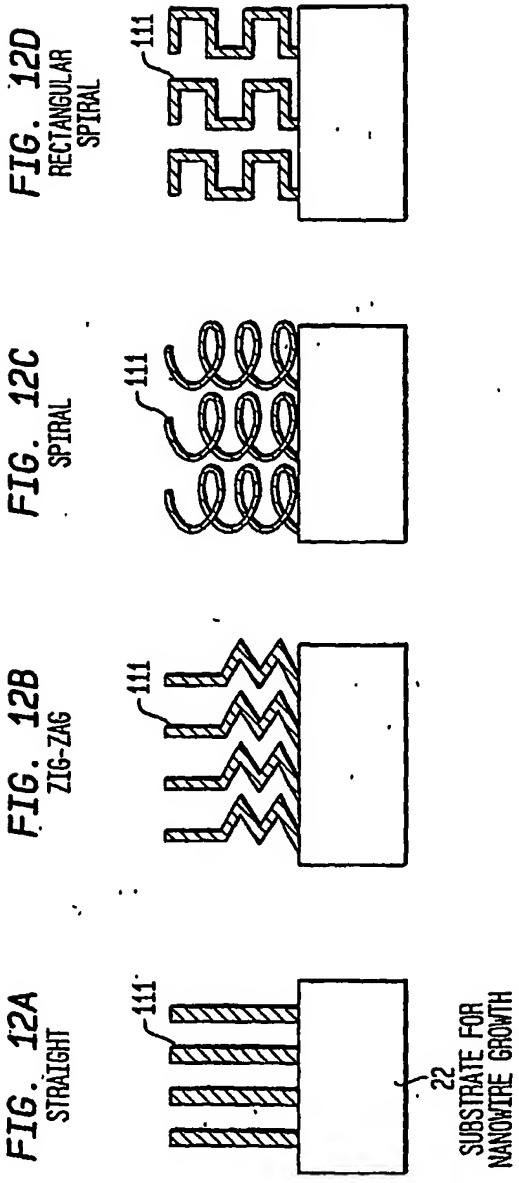


FIG. 12D
RECTANGULAR SPIRAL
111
FIG. 12C
SPIRAL
111
FIG. 12B
ZIG-ZAG
111
FIG. 12A
STRAIGHT
111
22
SUBSTRATE FOR NANOWIRE GROWTH

FIG. 13A

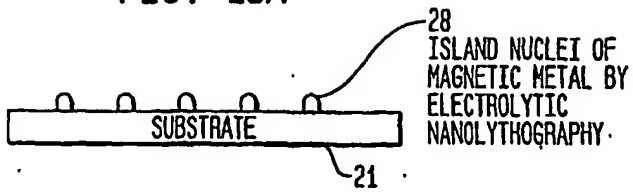


FIG. 13B

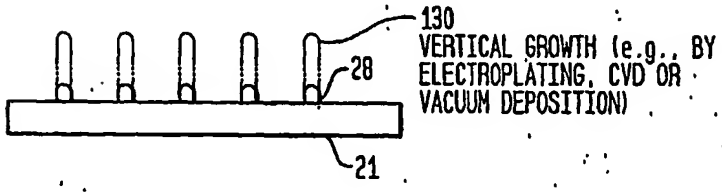


FIG. 13C

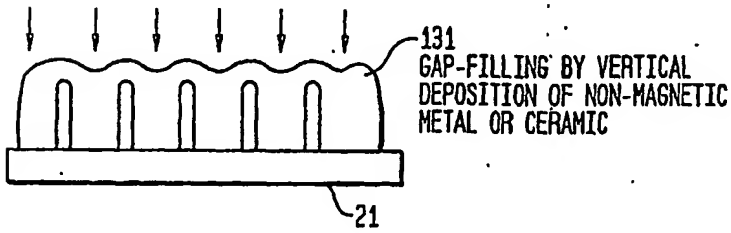


FIG. 13D

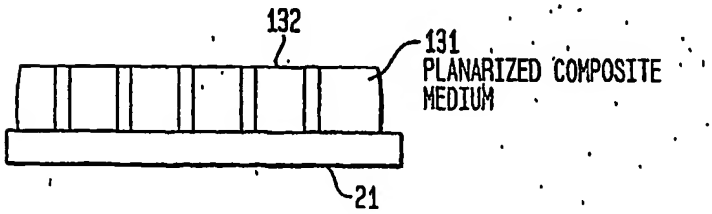


FIG. 14A

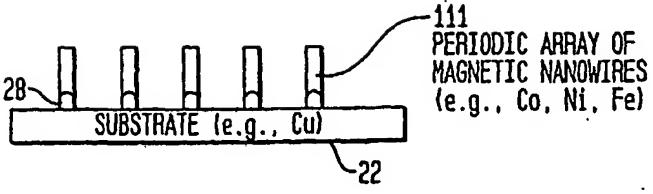


FIG. 14B
OXIDIZE OR CVD TO
FORM INSULATOR SKIN

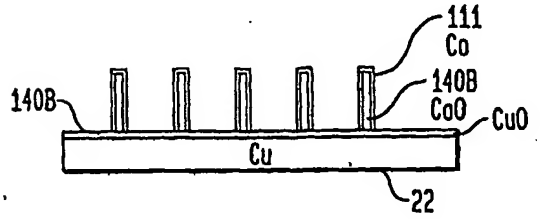


FIG. 14C
H_2 REDUCTION

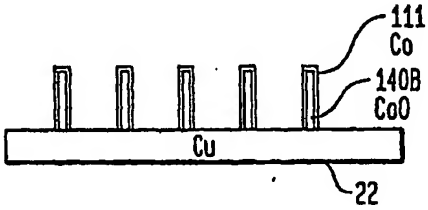


FIG. 14D
GAP-FILLING
ELECTRODEPOSITION

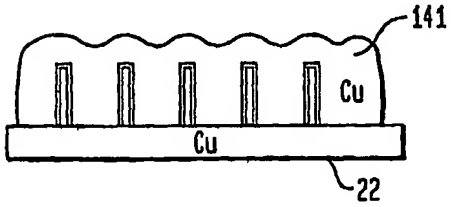


FIG. 14E
PLANARIZE
(e.g., BY CMP)

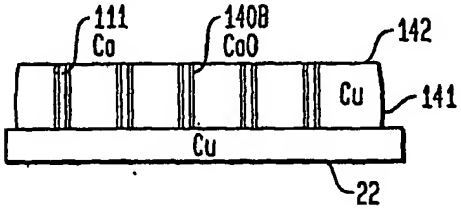


FIG. 15A

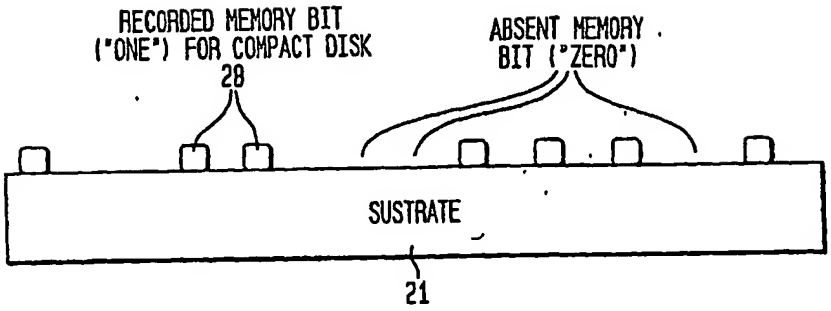


FIG. 15B

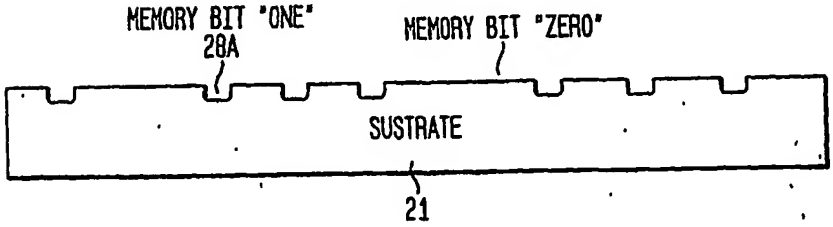


FIG. 16A

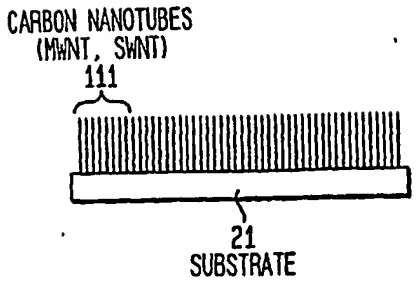


FIG. 16B

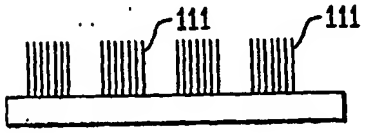


FIG. 16C

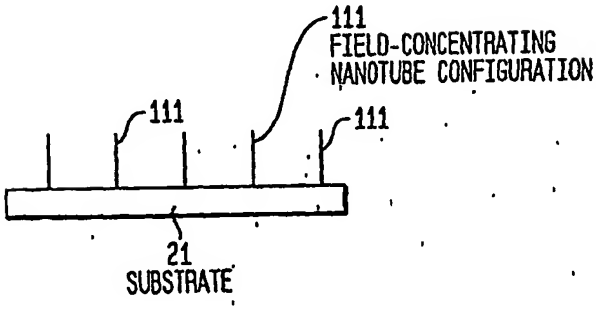


FIG. 16D

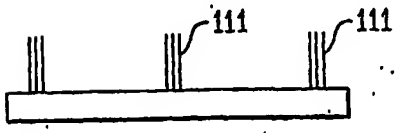
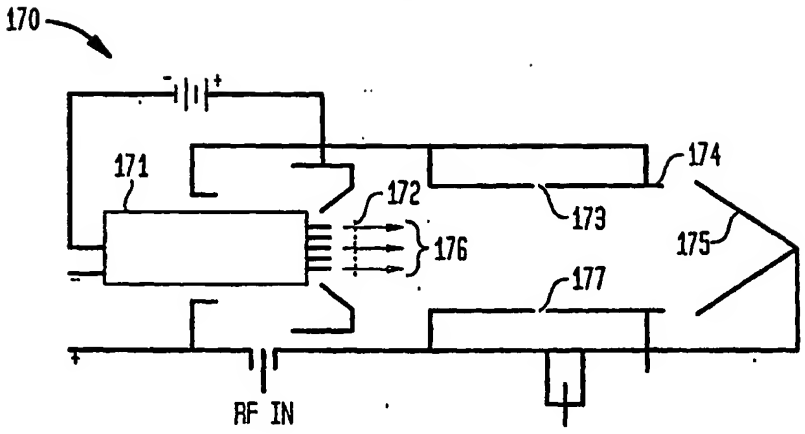


FIG. 17



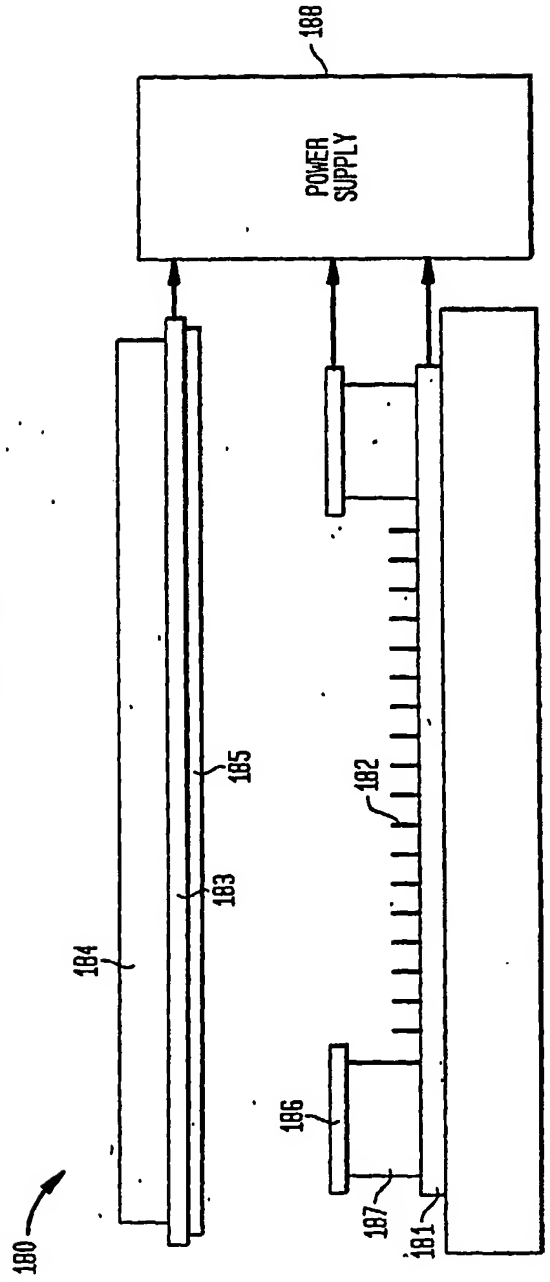


FIG. 18

FIG. 19

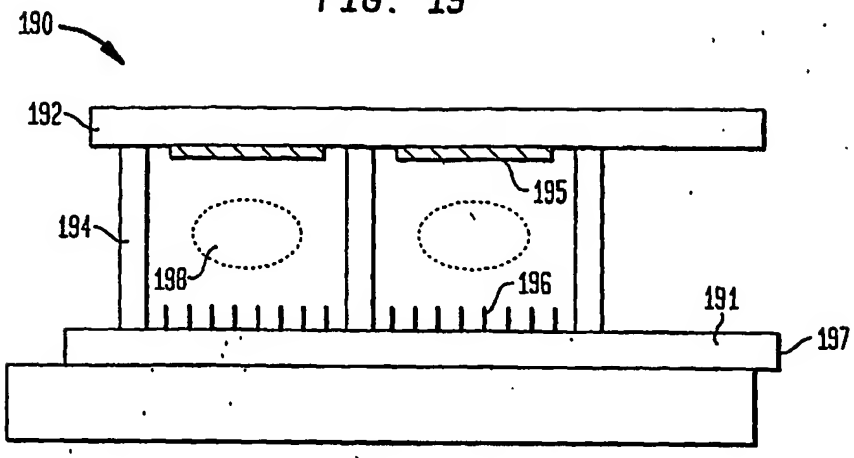

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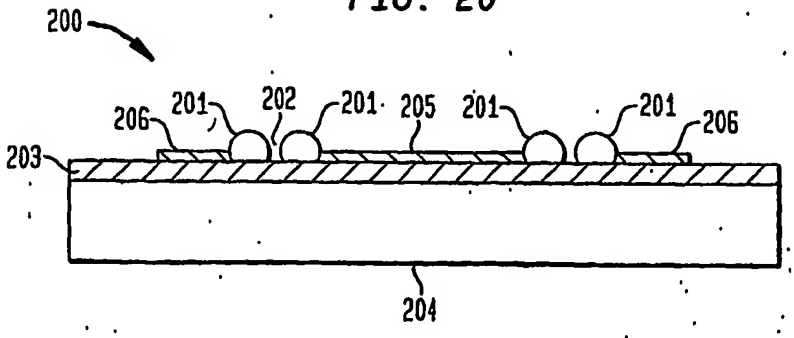
FIG. 20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